This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently amended) A receiver which converts a received signal directly to a baseband signal, comprising:

a switched-capacitor filter controlling a cutoff frequency when the baseband signal is filtered according to a control signal provided for a switched-capacitor element;

an oscillator generating a periodic signal;

a phase locked loop (PLL) circuit comprising a first divider, wherein the PLL circuit generates a periodic signal of a predetermined frequency according to an output signal from the first divider and the periodic signal generated by the oscillator; and

a second divider further dividing [[a]] the periodic signal generated by ~~said oscillator~~ the PLL circuit according to the received signal, wherein ~~characterized in that~~

[[an]] the output signal from the second divider is provided as the control signal for the switched-capacitor element.

2. (Currently amended) The receiver according to claim 1, wherein ~~characterized in that~~

said second divider is a programmable counter and is a divider in a system of a division to an integral multiple or a fractional-N system.

3. (Currently amended) The receiver according to claim 1, wherein ~~characterized in that~~

said switched-capacitor filter comprises at least an amplifier, and a resistor element, which functions as a feedback resistor of the amplifier[[,]] and is realized by the switched-capacitor element.

4. (Currently amended) A receiver which converts a received signal directly to a baseband signal, comprising:

an oscillator generating a periodic signal;

a mixer for mixing [[a]] the periodic signal generated by ~~said~~ the oscillator

with the received signal, and outputting a baseband signal;

a switched-capacitor filter controlling a cutoff frequency when filtering the baseband signal output from ~~said~~ the mixer according to a control signal provided for a switched-capacitor element;

a phase locked loop (PLL) circuit comprising a first divider, wherein the PLL circuit generates a periodic signal of a predetermined frequency according to an output signal from the first divider and the periodic signal generated by the oscillator; and

a second divider further dividing [[a]] the periodic signal generated by ~~said oscillator~~ the PLL circuit according to the received signal, wherein ~~characterized in that~~

the output signal from ~~said~~ the second divider is provided as the control signal for the switched-capacitor element.